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09/920,891	08/02/2001	Michael Kwan	A4231/T34410	9729

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APPLIED MATERIALS, INC.
2881 SCOTT BLVD. M/S 2061
SANTA CLARA, CA 95050

EXAMINER	
KACKAR, RAM N	

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/920,891
Filing Date: August 02, 2001
Appellant(s): KWAN ET AL.

Patrick M. Boucher
For Appellant

SUPPLEMENTAL EXAMINER'S ANSWER

This is in response to the REMAND TO THE EXAMINER dated 1/19/2004.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

The rejection of claims 17-22 stand or fall together.

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

5,990,000	*Hong et al*	*11-1999*
6,030,881	*Papasouliotis et al*	*02-2000*
6,268,274	*Wang et al*	*07-2001*
6,310,755	*Kholodenko et al*	*10-2001*
5,316,278	*Sherstinsky et al*	*05-1994*
5,937,323	*Orczyk et al*	*08-1999*

(10) Grounds of Rejection

The following ground(s) of rejection applicable to the appealed claims are restated in response to the requirements contained in the REMAND TO THE EXAMINER dated 1/19/2005 and accordingly as per option (2) Orczyk et al, Kholodenko et al and Sherstinsky et al are properly incorporated in the following grounds of rejection. No new grounds of rejection are included.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims17-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hong et al (US 5990000) in view of Papasouliotis et al (US 6030881) as evidenced by Orczyk et al (US 5937323), Kholodenko et al (US 6,310,755) and Sherstinsky et al (US 5,316,278).

Hong et al disclose a computer readable storage medium having a computer readable program embodied therein (See Col 6 line 58-65), for controlling the mixture of gases, chamber pressure, temperature, RF power level, pedestal position and other parameters of a process for deposition of a dielectric layer according to a three-step deposition/etch back/deposition process (See Fig 2A 230-245) so that it covers plurality of raised features and at least partially fills in gaps. (See Col 15 line 30-33).

Hong et al do not disclose that the deposition part of their three-step process could be a simultaneous deposition/Etch process. Consequently they do not disclose a mixture of deposition and inert gas and the ratio of deposition and sputter etch.

Papasouliotis et al disclose a multi step process using a mixture of deposition and an inert gas and teach that the ratio of deposition/etch for the simultaneous deposition and etch in first and third step, should be greater than 1 and preferably between 4 and 50 to ensure net deposition (Abstract and Col 4 line10-16).

There fore it would have been obvious to one of ordinary skill in the art at the time invention to modify the simple computer programmed deposition steps (Step 230 and 245 of Fig 2A) of Hong et al to simultaneous deposition/sputter steps by using a mixture of deposition and inert gas and maintain the ratio of Deposition/Sputter greater than 1 in order to have net deposition over gaps of high aspect ratios and be able to fill the bottom of the gap better before the closure of the gap at the top.

Regarding Claim 17 (c,d) and 20(g(iii-iv) Hong et al disclose a chemical etch step (Step 235 Fig 2A) after the first deposition step.

Hong et al disclose that deposition process is typically done at an elevated temperature (Col 4 line 24 and Fig 2A-Step 210). Orczyk et al also make the same observation (Col 1 line 30-34) that chemical vapor deposition typically requires elevated temperature.

Hong et al disclose an etch step after a deposition step (which is typically done at elevated temperature) but do not disclose a substrate-cooling step before starting gases for etching.

Papasouliotis et al disclose changing process parameters including changing temperature before transition from deposition to etching (Col 8 lines 42-45). Papasouliotis et al however do not explicitly disclose the temperature change step to be a cooling step.

Relation ship of deposition and etch to temperature is well known to people of ordinary skill in the art. Typical need for elevated temperature is discussed above. Typical need for cooling for temperature is discussed below.

Kholodenko et al teach (Col 1 lines 56-60) that in certain processes, it is also desirable to rapidly cool the substrate in order to maintain the substrate in a narrow range of temperatures especially for etching interconnect lines.

Sherstinsky et al (Col 1 lines15-26) also teach that in the plasma etching of semiconductor wafers, it is conventional to cool the wafer.

Therefore it would have been obvious to one having ordinary skill in the art at the time of invention to have an instruction to cool the substrate after a deposition step and before etch step so as to be able to control the substrate temperature properly for etch.

Since instruction for cooling step does not specify a temperature, duration or any other parameter for the control system it is assumed that those parameters could be adjusted by the operator at the process time. This means that if the etch temperature was no required to be low for a certain process, appropriate parameters with the instruction could make sure that there was no cooling but if some process needed active cooling, not having a cooling instruction to activate the control system would be disastrous. Therefore it would be obvious that having a cooling instruction would be better than not having it.

(11) Response to Argument

Status of prior art

During the fabrication of microcircuits on a semiconductor substrate, there is occasionally, a need to fill gaps of narrow widths and large depths (gaps with high aspect ratio-ratio of depth to width). Ordinary deposition tends to deposit more material at the corners. If allowed to continue, the deposition at corners prematurely closes the gap at top surface leaving unfilled hole underneath (Hong et al Fig 2C and 2D and Papasoliotis et al Fig 2A and 2B). In the prior art therefore, deposition step was followed by an etch (removal) step to selectively remove material at corners to open the hole from the top. This was then followed by another deposition step to fill the gap further. Sometimes several iterations of these steps was needed to satisfactorily close the gap. As aspect ratio have become even higher, above process has been found deficient.

Papasoliotis et al have found that a modified deposition step having simultaneous deposition and etch is beneficial in this situation. Ratio of deposition/etch determines net deposition or net removal of material. Papasoliotis et al have disclosed the steps of this process

without being too process specific. They have disclosed that transition of a deposition step to an etch step may in general be accompanied by change of process parameters including the temperature.

Response to Argument

Applicant argues that neither Hong nor Papasouliotis teach or suggest a separate cooling step. Applicant further argues that in Papasoliotis the reference to change of temperature at the transition from deposition to etch is not equivalent to a cooling step and in Sherstinsky and Kholodenko the cooling step in reference to etching is for the purpose of maintaining a temperature rather than reducing the temperature.

Papasoliotis et al indicate that in general, a change of temperature may be required after deposition in preparation for the etch. Considering this in view of the knowledge (Hong and Orczyk et al) that, plasma deposition in general is accompanied by an elevation in temperature while etching needs cooling the substrate, even if to maintain substrate at a lower temperature, it would have been obvious that in general a cooling step after deposition may be needed in preparation for etching, at least in case, change of temperature in Papasoliotis turns out to be cooling for a specific process. It should be understood that "cooling step" sets up the hardware for cooling and the amount of cooling may be controlled by parameters like time and temperature in a feed back control. Therefore actual cooling required could be controlled from zero to any significant value.

Secondly, as taught by Sherstinsky and Kholodenko etching step may need cooling, at least for maintaining the substrate at a low temperature. As plasma and ion bombardment is the cause of substrate heat during etch, it would be obvious and prudent to make sure that the

cooling system is ready before plasma is turned on for etching since, cooling is never instantaneous.

Regarding applicant remarks about the word "thereafter" in the claim language, it does not appear that this means that the cooling step is completed before etchant gases are started so that during flow of etchant gases and etching no cooling system may be in operation.

Cooling the substrate could also be implied (at least for claim 17c), since after deposition and before any other step substrate left to itself will tend to cool without doing any thing.

Moreover, transposition of process steps or the splitting of steps has been held obvious (*Ex Parte Rubin* 128 USPQ 440) and so is performance of two steps simultaneously (*In re Tatincloux* 108 USPQ 125 (CCPA 1955)).

Applicant further argues that there is no motivation to combine Hong with Papasoliotis in the manner suggested and because of differences in PECVD and HDP-CVD there is no reasonable expectation of success.

Hong et al teach the use of computer with memory and instructions to execute a Deposition/Etch/Deposition process using PECVD and suggest that induction coupled HDP device could equally benefit from Dep/Etch/Dep process controlled by the computer (Col 5 lines 28-30). Papasoliotis et al on the other hand disclose the advantage of HDP and simultaneous dep/etch for filling gaps of high aspect ratio. Nothing they say amounts to leading away from the invention.

In view of this, applicant's suggestion that there was even a hint of teaching away and less than reasonable expectation of success is in correct

In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

RK
January 31, 2005

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